

## N-Channel 100V(D-S) MOSFET

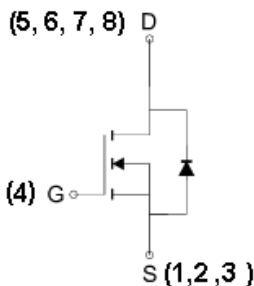
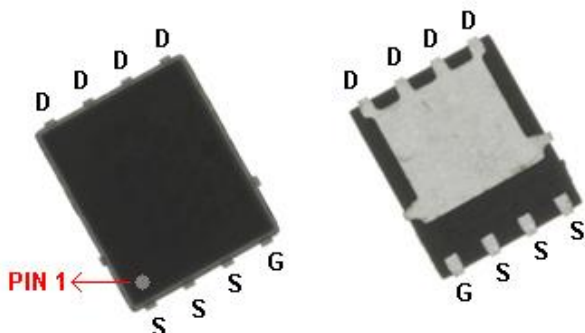
### GENERAL DESCRIPTION

The MEE72962-G is a N-Channel enhancement mode power field effect transistor, using Force-MOS patented Extended Trench Gate (ETG) technology. This advanced technology is especially tailored to minimize on state resistance and gate charge, and enhance avalanche capability. These devices are particularly suited for medium voltage application such as charger, adapter, notebook computer power management and other lighting dimming powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

### PIN CONFIGURATION

(PowerDFN 5x6)

Top View



N-Channel MOSFET

Ordering Information: MEE72962-G (Green product- Halogen free)

### Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V <sub>DSS</sub>	100	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current*	I <sub>D</sub>	T <sub>C</sub> =25°C	47
		T <sub>C</sub> =70°C	37
		T <sub>A</sub> =25°C	11
		T <sub>A</sub> =70°C	9
Pulsed Drain Current	I <sub>DM</sub>	140	140
Maximum Power Dissipation*	P <sub>D</sub>	T <sub>C</sub> =25°C	48
		T <sub>C</sub> =70°C	31
		T <sub>A</sub> =25°C	3
		T <sub>A</sub> =70°C	2
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Thermal Resistance-Junction to Case *	R <sub>θJC</sub>	2.6	°C/W
Thermal Resistance-Junction to Ambient*	R <sub>θJA</sub>	45	°C/W

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

\*Chip silicon limitation current is 100A

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**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	100			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	1		3	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$			1	$\mu A$
$R_{DS(ON)}$	Drain-Source On-State Resistance <sup>a</sup>	$V_{GS}=10V, I_D=20A$		8.5	10.5	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$		12.5	16.5	
$V_{SD}$	Diode Forward Voltage	$I_S=1A, V_{GS}=0V$			1	V
<b>DYNAMIC</b>						
$Q_g$	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V, I_D=20A$		49.2		nC
$Q_g$	Total Gate Charge	$V_{DS}=50V, V_{GS}=4.5V, I_D=20A$		26.8		
$Q_{gs}$	Gate-Source Charge			16		
$Q_{gd}$	Gate-Drain Charge			10.3		
$C_{iss}$	Input capacitance	$V_{DS}=30V, V_{GS}=0V, f=1.0MHz$		2819		pF
$C_{oss}$	Output Capacitance			868		
$C_{rss}$	Reverse Transfer Capacitance			55		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=50V, R_L=2.5\ \Omega$ $V_{GS}=10V, R_G=6\ \Omega$ $I_D=20A$		25.9		ns
$t_r$	Turn-On Rise Time			69.5		
$t_{d(off)}$	Turn-Off Delay Time			57.2		
$t_f$	Turn-Off Fall Time			24		

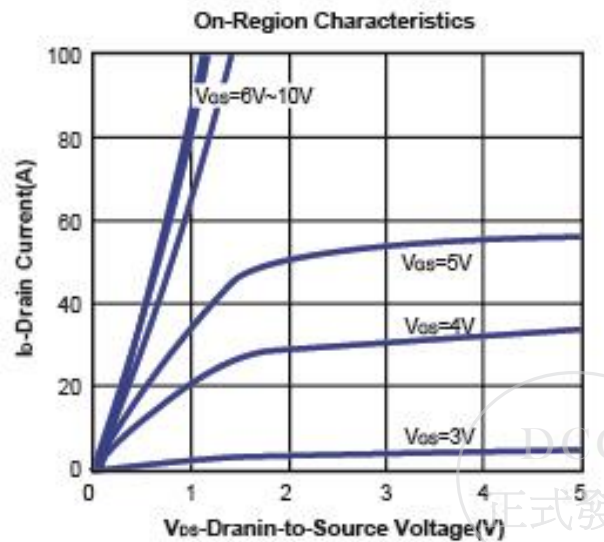
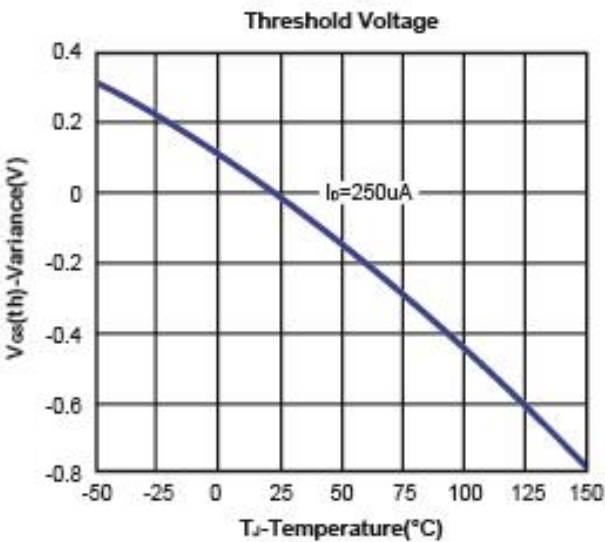
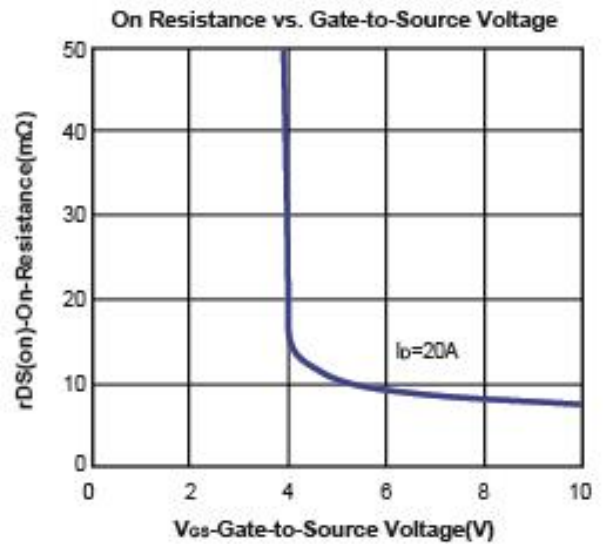
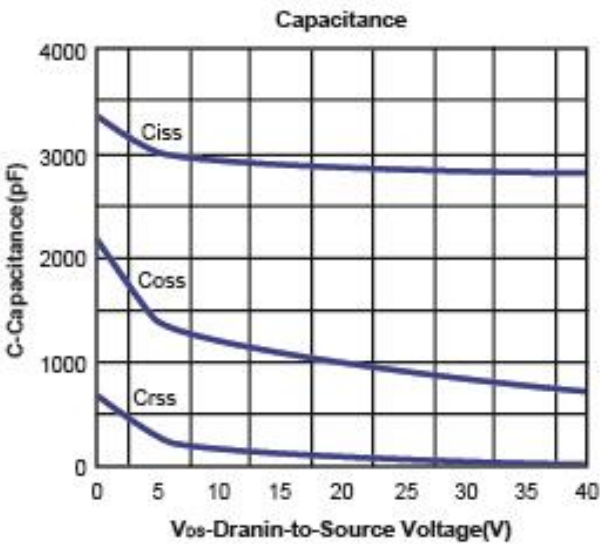
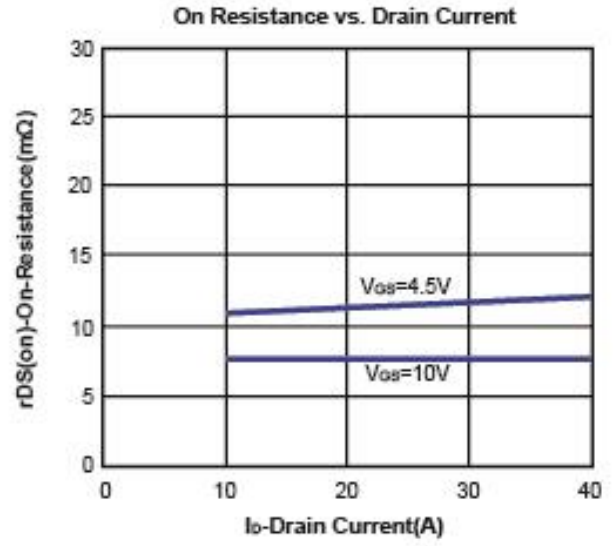
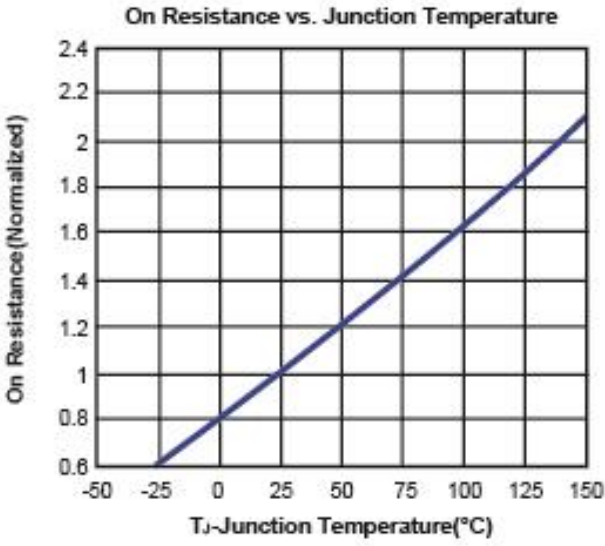
Notes: a. Pulse test: pulse width  $\leq 300\ \mu s$ , duty cycle  $\leq 2\%$ , Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.



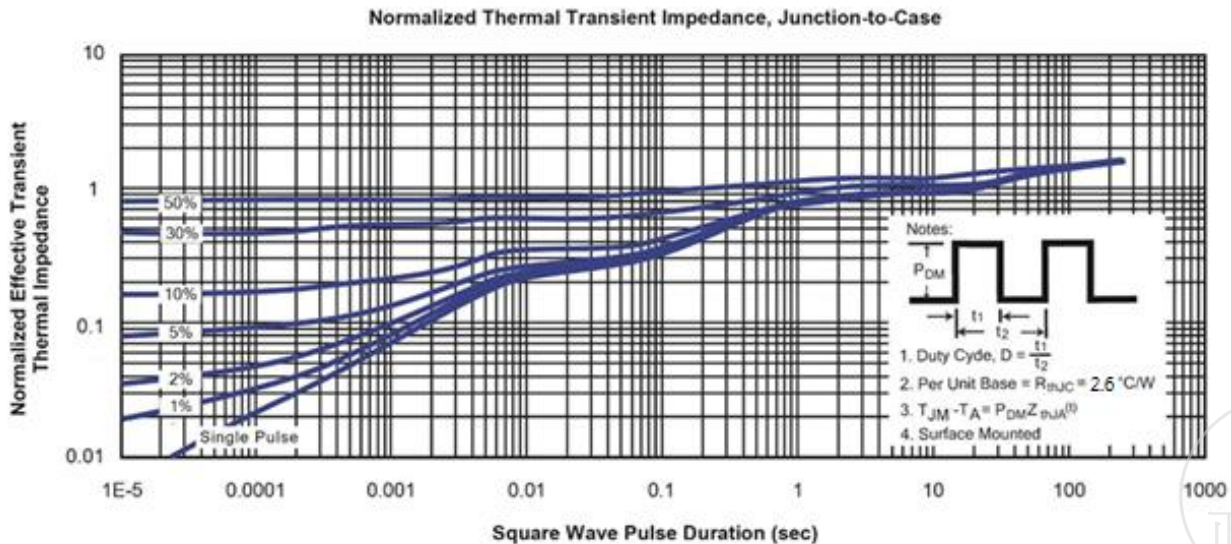
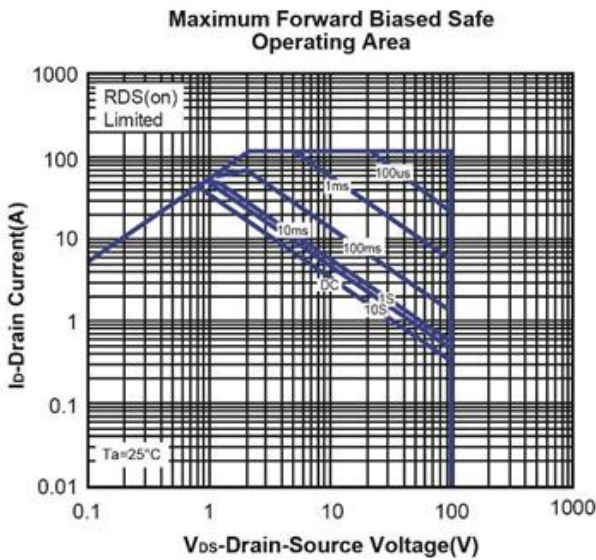
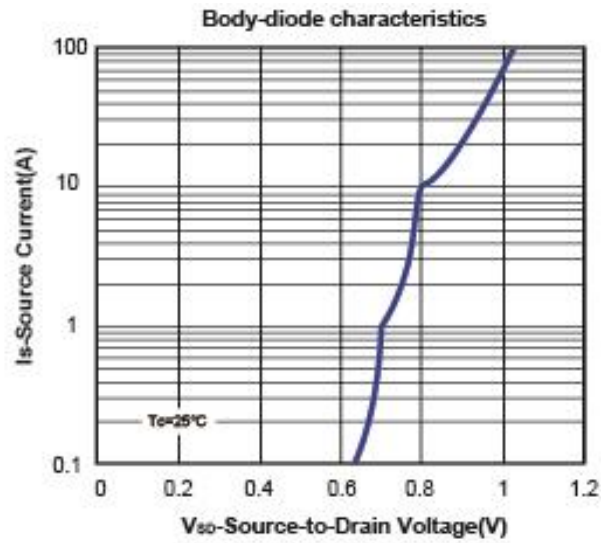
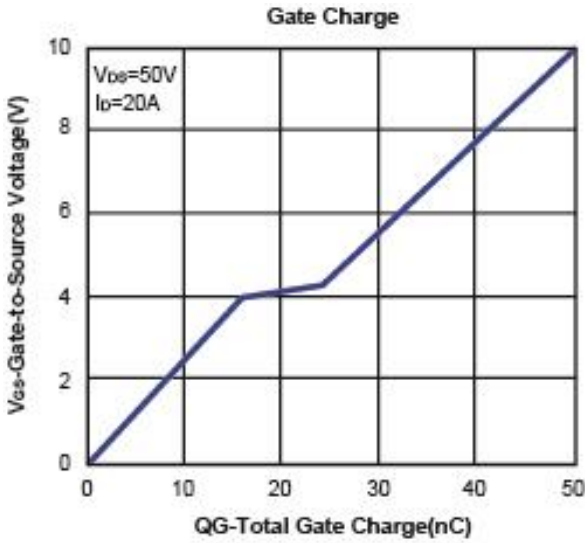
## N-Channel 100V(D-S) MOSFET

Typical Characteristics (T<sub>J</sub> = 25°C Noted)



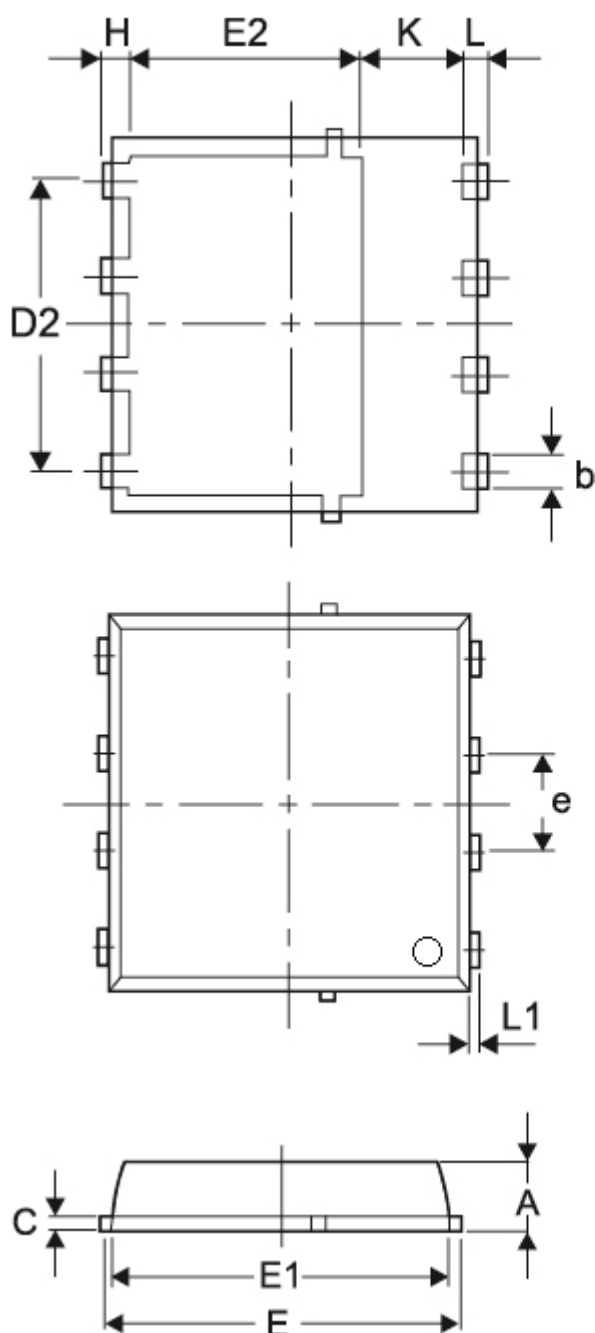
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#### PowerDFN 5x6 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.25
b	0.33	0.51
C	0.155	0.30
D1	4.80	5.00
D2	3.61	3.96
E	5.8	6.20
E1	5.6	5.90
E2	3.35	4.31
e	1.27 BSC	
H	0.35	0.61
K	1.60	-
L	0.35	0.71
L1	0.05	0.20

